

# Ultra High-PSRR, Low-Noise, 300mA CMOS Linear Regulator

## General Description

The FC8130 features ultra-high power supply rejection ratio, low output voltage noise, low dropout voltage, low quiescent current and fast transient response. It guarantees delivery of 300mA output current and supports preset output voltages ranging from 0.8V to 4.0 V with 0.1V increment.

Based on its low quiescent current consumption and its less than 1uA shutdown mode of logical operation, the FC8130 is ideal for battery-powered applications. The high power supply rejection ratio of the FC8130 holds well for low input voltages typically encountered in battery-operated systems. The regulator is stable with small ceramic capacitive loads (1μF typical).

The FC8130 is available in miniature SOT-23-5, uDFN-4, SC-70-5 and SC-82-4 package.

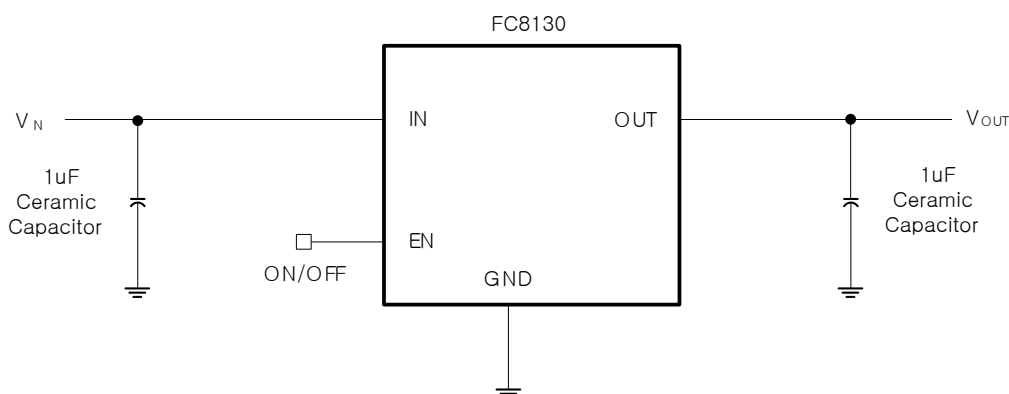
## Applications

- Wireless handsets
- PCMCIA cards
- DSP core power
- Hand-held instruments
- Battery-powered systems
- Portable information appliances

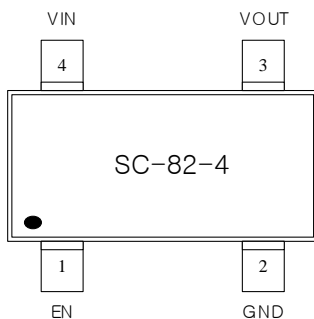
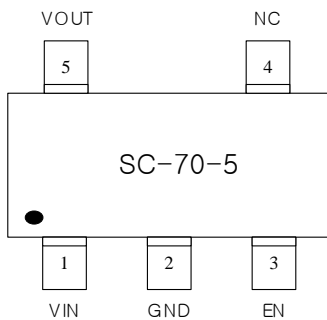
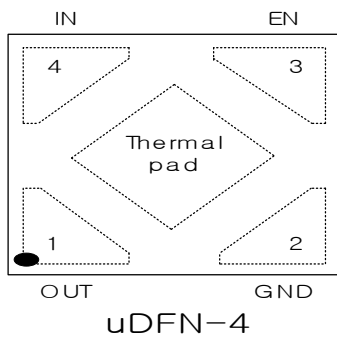
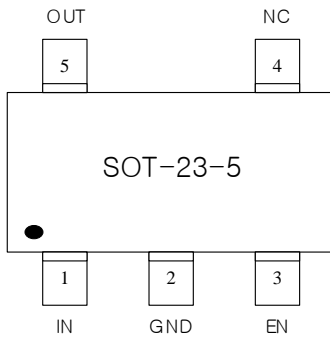
## Features

- 300mA guaranteed output current
- 75dB typical PSRR at 1kHz
- 260mV ( $V_{OUT}=3.3V$ ) typical dropout at 300mA
- 52μA typical quiescent current
- Less than 1μA typical shutdown mode
- Fast line and load transient response
- 1.7V to 5.5V input range
- Auto-discharge during chip disable
- 0.8V to 4.0V output voltage range
- Stable with small ceramic output capacitors
- Fold-back over current protection
- ±1% output voltage tolerance

## Typical Application



## Connection Diagrams



## Order information

FC8130-XXVN05NRR

XX Output voltage

VN05 SOT-23-5 Package

NRR RoHS & Halogen free package  
Rating: -40 to 85°C  
Package in Tape & Reel

FC8130-XXFJ04NRR

XX Output voltage

FJ04 uDFN-4 Package

NRR RoHS & Halogen free package  
Rating: -40 to 85°C  
Package in Tape & Reel

FC8130-XXVI05NRR

XX Output voltage

VI05 SC-70-5 Package

NRR RoHS & Halogen free package  
Rating: -40 to 85°C  
Package in Tape & Reel

FC8130-XXVJ04NRR

XX Output voltage

VI05 SC-82-4 Package

NRR RoHS & Halogen free package  
Rating: -40 to 85°C  
Package in Tape & Reel

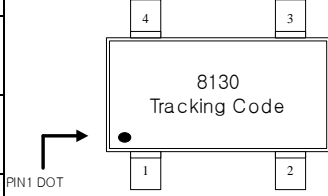
## Order, Marking & Packing Information

Package	Vout	Product ID.	Marking	Packing
SOT-23-5	0.8V	FC8130-08VN05NRR		Tape & Reel 3Kpcs
	1.0V	FC8130-10VN05NRR		
	1.2V	FC8130-12VN05NRR		
	1.3V	FC8130-13VN05NRR		
	1.5V	FC8130-15VN05NRR		
	1.8V	FC8130-18VN05NRR		
	2.5V	FC8130-25VN05NRR		
	2.8V	FC8130-28VN05NRR		
	3.0V	FC8130-30VN05NRR		
	3.3V	FC8130-33VN05NRR		

Package	Vout	Product ID.	Marking	Packing
uDFN-4	0.8V	FC8130-08FJ04NRR	 X X = tracking code	Tape & Reel 8Kpcs
	1.0V	FC8130-10FJ04NRR	 X X = tracking code	
	1.2V	FC8130-12FJ04NRR	 X X = tracking code	
	1.3V	FC8130-13FJ04NRR	 X X = tracking code	
	1.5V	FC8130-15FJ04NRR	 X X = tracking code	

	1.8V	FC8130-18FJ04NRR	 X X = tracking code	
	2.5V	FC8130-25FJ04NRR	 X X = tracking code	
	2.8V	FC8130-28FJ04NRR	 X X = tracking code	
	3.0V	FC8130-30FJ04NRR	 X X = tracking code	
	3.3V	FC8130-33FJ04NRR	 X X = tracking code	

Package	Vout	Product ID.	Marking	Packing
SC-70-5	0.8V	FC8130-08VI05NRR		Tape & Reel 3Kpcs
	1.0V	FC8130-10VI05NRR		
	1.2V	FC8130-12VI05NRR		
	1.3V	FC8130-13VI05NRR		
	1.5V	FC8130-15VI05NRR		
	1.8V	FC8130-18VI05NRR		
	2.5V	FC8130-25VI05NRR		
	2.8V	FC8130-28VI05NRR		
	3.0V	FC8130-30VI05NRR		
	3.3V	FC8130-33VI05NRR		

Package	Vout	Product ID.	Marking	Packing
SC-82-4	0.8V	FC8130-08VJ04NRR		Tape & Reel 3Kpcs
	1.0V	FC8130-10VJ04NRR		
	1.2V	FC8130-12VJ04NRR		
	1.3V	FC8130-13VJ04NRR		
	1.5V	FC8130-15VJ04NRR		
	1.8V	FC8130-18VJ04NRR		
	2.5V	FC8130-25VJ04NRR		
	2.8V	FC8130-28VJ04NRR		
	3.0V	FC8130-30VJ04NRR		
	3.3V	FC8130-33VJ04NRR		

## Pin Functions

Name	SOT-23-5	uDFN-4	SC-70-5	SC-82-4	Function
IN	1	4	1	4	Supply Voltage Input. Require a minimum input capacitor of close to 1uF ceramic capacitor to ensure stability and sufficient decoupling from the ground pin.
GND	2	2	2	2	Ground Pin.
EN	3	3	3	1	Enable Input. Enable the regulator by pulling the EN pin High. To keep the regulator on during normal operation, connect the EN pin to $V_{IN}$ . The EN pin must not exceed $V_{IN}$ under all operating conditions.
NC	4	N/A	4	N/A	No Connected.
OUT	5	1	5	3	Regulated Output Voltage Pin. A small 1uF ceramic capacitor is needed from this pin to ground to assure stability.
Thermal Pad	N/A	YES	N/A	N/A	The thermal pad with large thermal land area on the PCB will help chip power dissipation, to connect it to GND together normally.

## Functional Block Diagram

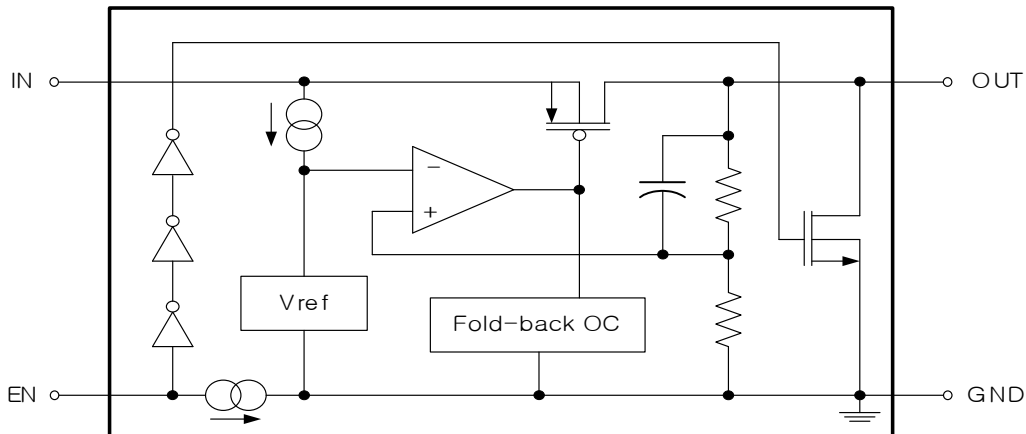


FIG.1. Functional Block Diagram of FC8130



# FC8130

## Absolute Maximum Ratings (Notes 1, 2)

IN, EN, OUT	-0.3V to 6.5V	Lead Temperature ( Soldering, 10 sec.)	260°C
Power Dissipation	(Note 6)	ESD Rating	
Storage Temperature Range	-65°C to 150°C	Human Body Mode I	2KV
Junction Temperature (T <sub>J</sub> )	150°C	Machine Model	200V

## Operating Ratings (Note 1, 2)

Supply Voltage	1.7V to 5.5V	Operating Temperature Range	-40°C to 85°C
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## Thermal Resistance:

Symbol	θ <sub>JA</sub> (Note 3)	θ <sub>Jc</sub> (Note 4)
SOT-23-5	152(°C/W)	81(°C/W)
uDFN-4	110(°C/W)	23(°C/W)
SC-70-5	331(°C/W)	115 (°C/W)
SC-82-4	331(°C/W)	115 (°C/W)

## Electrical Characteristics

Unless otherwise specified, all limits guaranteed for V<sub>N</sub> = V<sub>OUT</sub> +1V (Note 5), V<sub>EN</sub>=V<sub>N</sub>, C<sub>N</sub> = C<sub>OUT</sub> = 1μF, T<sub>A</sub> = 25°C. Boldface limits apply for the operating temperature extremes: -40°C and 85°C.

Symbol	Parameter	Conditions	Min	Typ (Note 7)	Max	Units
V <sub>IN</sub>	Input Voltage		1.7		5.5	V
V <sub>OUT</sub>	Output Voltage		0.8		4.0	V
Δ V <sub>OTL</sub>	Output Voltage Tolerance	V <sub>out</sub> > 2.0V, T=25°C	X0.99		X1.01	V
		V <sub>out</sub> < =2.0V, T=25°C	-20		+20	mV
		V <sub>out</sub> >2V, -40~85°C	X0.97		X1.03	V
		V <sub>out</sub> < =2V, -40~85°C	-60		60	mV
I <sub>OUT</sub>	Maximum Output Current	Average DC Current Rating	300			mA
I <sub>cl</sub>	Current Limit	V <sub>in</sub> =V <sub>out</sub> +1V		420		mA
I <sub>sc</sub>	Short Current Limit			40		mA
I <sub>q</sub>	Quiescent C urrent	I <sub>OUT</sub> = 0mA		52	75	μA
I <sub>SD</sub>	Shutdown Supply Current	V <sub>OUT</sub> = 0V, EN = GND		0.2	1	μA
V <sub>DO</sub>	Dropout Voltage (Note 5)	I <sub>OUT</sub> = 300mA, V <sub>out</sub> =0.8V		860		mV
		I <sub>OUT</sub> = 300mA, V <sub>out</sub> =1.2V		580		
		I <sub>OUT</sub> = 300mA, V <sub>out</sub> =1.5V		440		
		I <sub>OUT</sub> = 300mA, V <sub>out</sub> =1.8V		380		
		I <sub>OUT</sub> = 300mA, V <sub>out</sub> =2.8V		290		
		I <sub>OUT</sub> = 300mA, V <sub>out</sub> =3.3V		260		
Δ V <sub>OUT</sub>	Line Regulation	I <sub>OUT</sub> = 1mA, (V <sub>OUT</sub> + 1V) ≤ V <sub>N</sub> ≤ 5.5V		0.02	0.1	%/V
	Load Regulation	1mA ≤ I <sub>OUT</sub> ≤ 300mA		10	30	mV
PSRR	Power supply rejection ratio	f = 1kHz, Ripple 0.2 V <sub>p-p</sub> , V <sub>in</sub> =Set V <sub>out</sub> +1V, I <sub>out</sub> = 30mA		75		dB
e <sub>n</sub>	Output Voltage Noise	V <sub>OUT</sub> =0.8V, I <sub>OUT</sub> =30mA, 10Hz ≤ f ≤ 100kHz		40		μV <sub>RMS</sub>
V <sub>EN</sub>	EN Input Threshold		1.0			V
					0.4	



# FC8130

$I_{EN}$	EN Input Bias Current	EN=GND or VIN		0.1	1	$\mu A$
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Note 1: Absolute Maximum ratings indicate limits beyond which damage may occur. Electrical specifications do not apply when operating the device outside of its rated operating conditions.

Note 2: All voltages are with respect to the potential at the ground pin.

Note 3:  $\theta_{JA}$  is measured in the natural convection at  $T_A=25^\circ C$  on a high effective thermal conductivity test board (2 layers, 2S0P).

Note 4:  $\theta_{JC}$  represents the resistance to the heat flows the chip to package top case

Note 5: Dropout voltage is measured by reducing  $V_{IN}$  until  $V_{OUT}$  drops 100mV from its nominal value at  $V_N - V_{OUT} = 1V$ .

Note 6: Maximum Power dissipation for the device is calculated using the following equations:

$$P_D = \frac{T_{J(MAX)} - T_A}{\theta_{JA}}$$

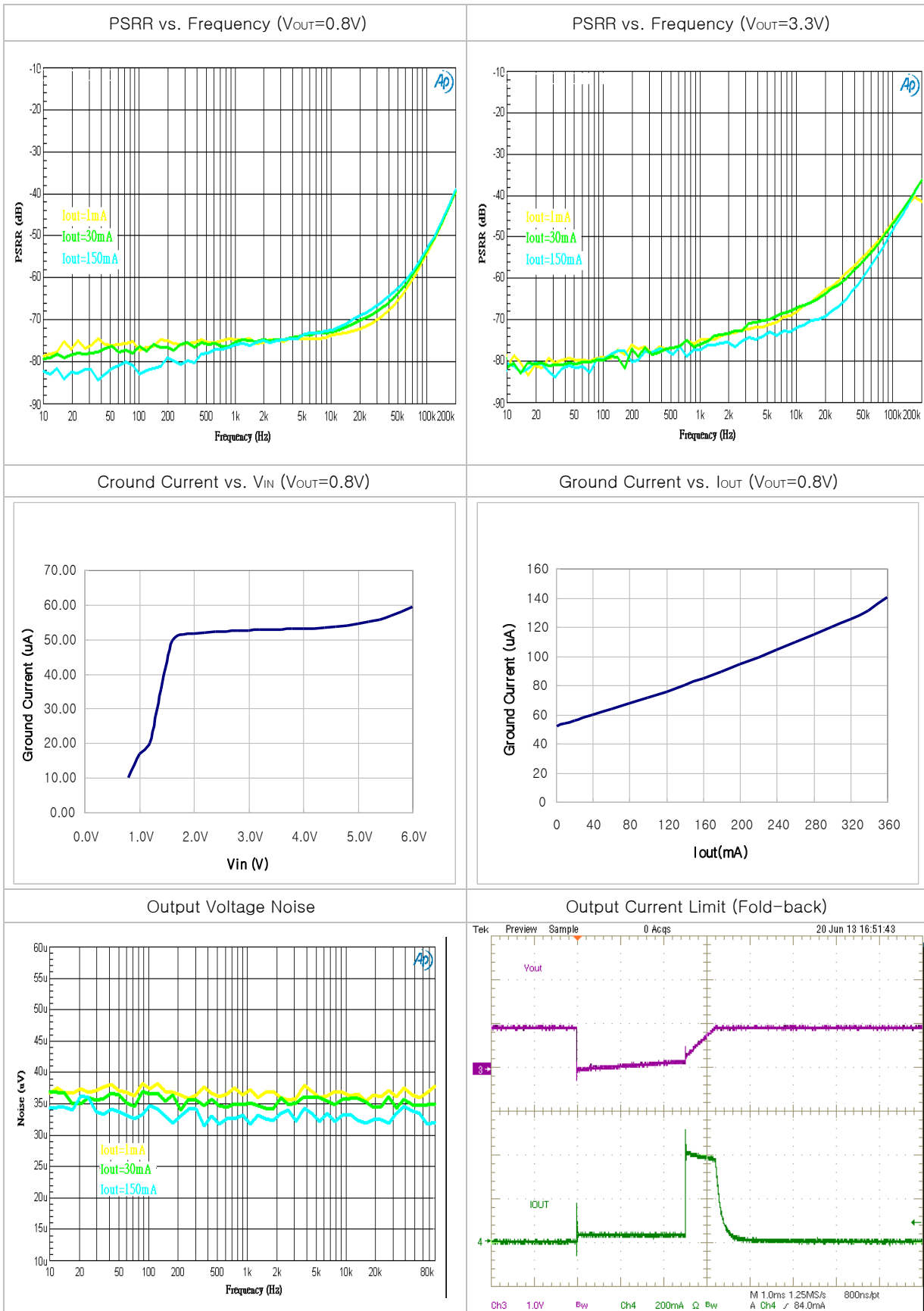
Where  $T_{J(MAX)}$  is the maximum junction temperature,  $T_A$  is the ambient temperature, and  $\theta_{JA}$  is the junction -to-ambient thermal resistance. E.g. for the SOT-23-5 package  $\theta_{JA} = 152^\circ C/W$ ,  $T_{J(MAX)} = 150^\circ C$  and using  $T_A = 25^\circ C$ , the maximum power dissipation is found to be 0.82W. The derating factor ( $-1/\theta_{JA}$ ) =  $-6.6mW/^\circ C$ , thus below  $25^\circ C$  the power dissipation figure can be increased by 6.6mW per degree, and similarly decreased by this factor for temperatures above  $25^\circ C$ .

Note 7: Typical values represent the most likely parametric norm.



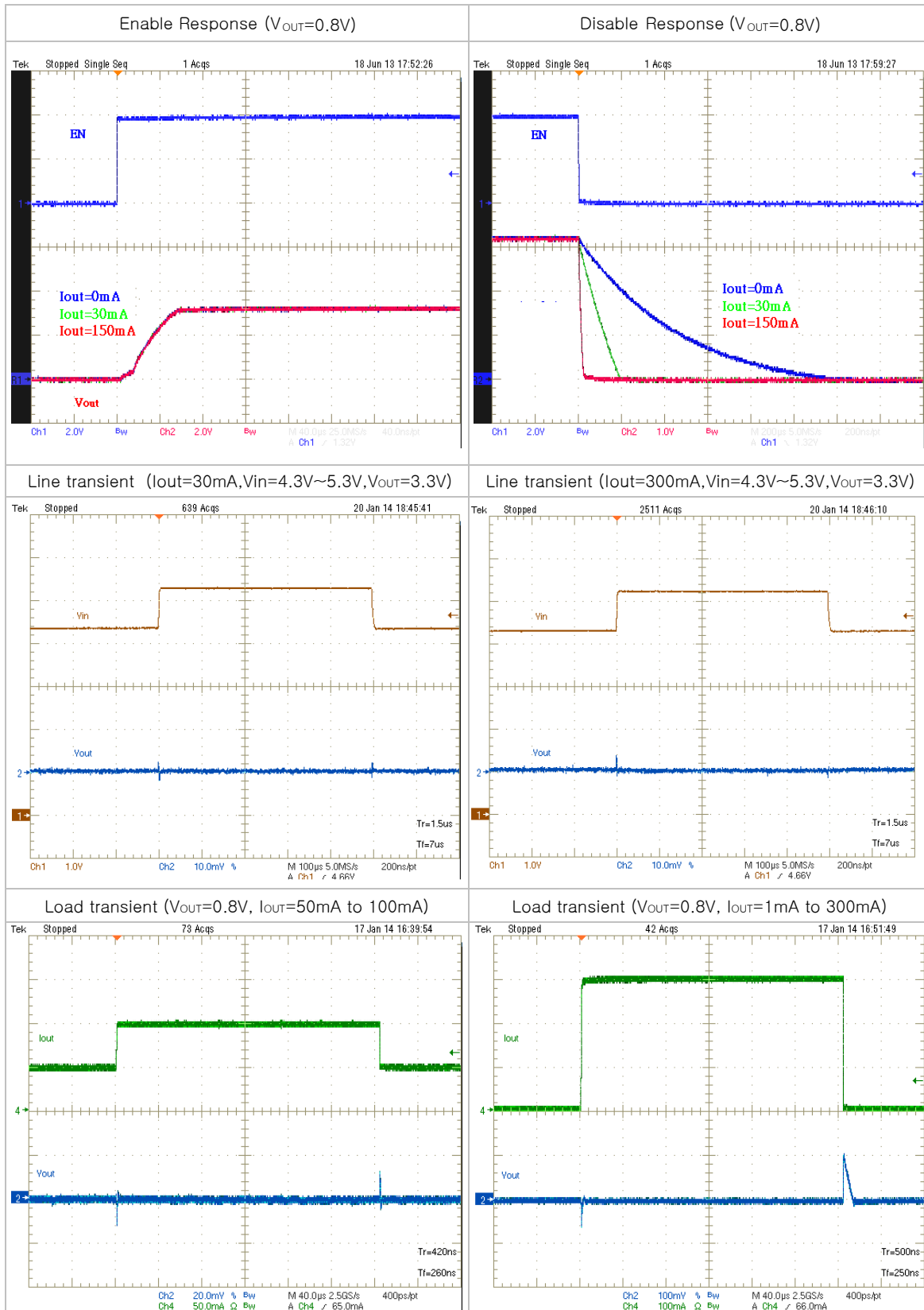
## Typical Performance Characteristics

Unless otherwise specified,  $V_{IN} = V_{OUT(NOM)} + 1V$ ,  $V_{EN}=V_{IN}$ ,  $C_{IN} = C_{OUT} = 1\mu F$ ,  $T_A = 25^\circ C$



## Typical Performance Characteristics (cont.)

Unless otherwise specified,  $V_N = V_{OUT(NOM)} + 1V$ ,  $V_{EN} = V_N$ ,  $C_N = C_{OUT} = 1\mu F$ ,  $T_A = 25^\circ C$





## Application Information

### General Description

Referring to Fig.1 as shown in the Functional Block Diagram section, the FC8130 adopts the classical regulator topology in which negative feedback control is used to perform the desired voltage regulating function. The sub  $V_{out}$ -select form the feedback circuit which samples the output voltage for the error amplifier's non-inverting input. The inverting input is set to the bandgap reference voltage. Due to its high open-loop gain, the error amplifier ensures that the sampled output feedback voltage at its non-inverting input is virtually equal to the preset voltage reference voltage. The error amplifier compares the voltage difference at its inputs and produces an appropriate driving voltage to the P-channel MOS pass transistor, which controls the amount of current reaching the output. If there are changes in the output voltage due to load changes, the feedback resistors register these changes to the non-inverting input of the error amplifier. The error amplifier then adjusts its driving voltage to maintain virtual short between its two input nodes under all loading conditions. The regulation of the output voltage is achieved as a direct result of the error amplifier keeping its input voltages equal. This negative feedback control topology is further augmented by the shutdown, the temperature and current protection circuitry.

### Output Capacitor

The FC8130 is specially designed for use with ceramic output capacitors of as low as  $1\mu\text{F}$  to take advantage of the savings in cost and space, as well as the superior filtering of high frequency noise. Capacitors of higher value or other types may be used, but it is important to make sure its equivalent series resistance (ESR) be restricted to less than  $0.5\Omega$ . The use of larger capacitors with smaller ESR values is desirable for applications involving large and fast input or output transients, as well as situations where the application systems are not physically located immediately adjacent to the battery power source. Typical ceramic capacitors suitable for use with the FC8130 are X5R and X7R. The X5R and the X7R capacitors are able to maintain their capacitance values to within  $\pm 20\%$  and  $\pm 10\%$ , respectively, as the temperature increases.

### No-Load Stability

The FC8130 is capable of stable operation during no-load conditions, a mandatory feature for some applications such as CMOS RAM keep-alive operations.

### Input Capacitor

A minimum input capacitance of  $1\mu\text{F}$  is required for FC8130. The capacitor value may be increased without limit. Improper workbench set-ups may have adverse effects on the normal operation of the regulator. A case in point is the instability that may result from long supply lead inductance coupling to the output through the gate capacitance of the pass transistor. This will establish a pseudo LCR network, and is likely to happen under high current conditions or near dropout. A  $10\mu\text{F}$  tantalum input capacitor will dampen the parasitic LCR action thanks to its high ESR. However, cautions should be exercised to avoid regulator short-circuit damage when tantalum capacitors are used, for they are prone to fail in short-circuit operating conditions.



## Power Dissipation

Thermal overload results from excessive power dissipation that causes the IC junction temperature to increase beyond a safe operating level. The concept of thermal resistance  $\theta_{JA}$  ( $^{\circ}\text{C}/\text{W}$ ) is often used to describe an IC junction's relative readiness in allowing its thermal energy to dissipate to its ambient air. An IC junction with a low thermal resistance is preferred because it is relatively effective in dissipating its thermal energy to its ambient, thus resulting in a relatively low and desirable junction temperature. The relationship between  $\theta_{JA}$  and  $T_J$  is as follows:

$$T_J = \theta_{JA} \times (P_D) + T_A$$

$T_A$  is the ambient temperature, and  $P_D$  is the power generated by the IC and can be written as:

$$P_D = I_{OUT}(V_{IN} - V_{OUT})$$

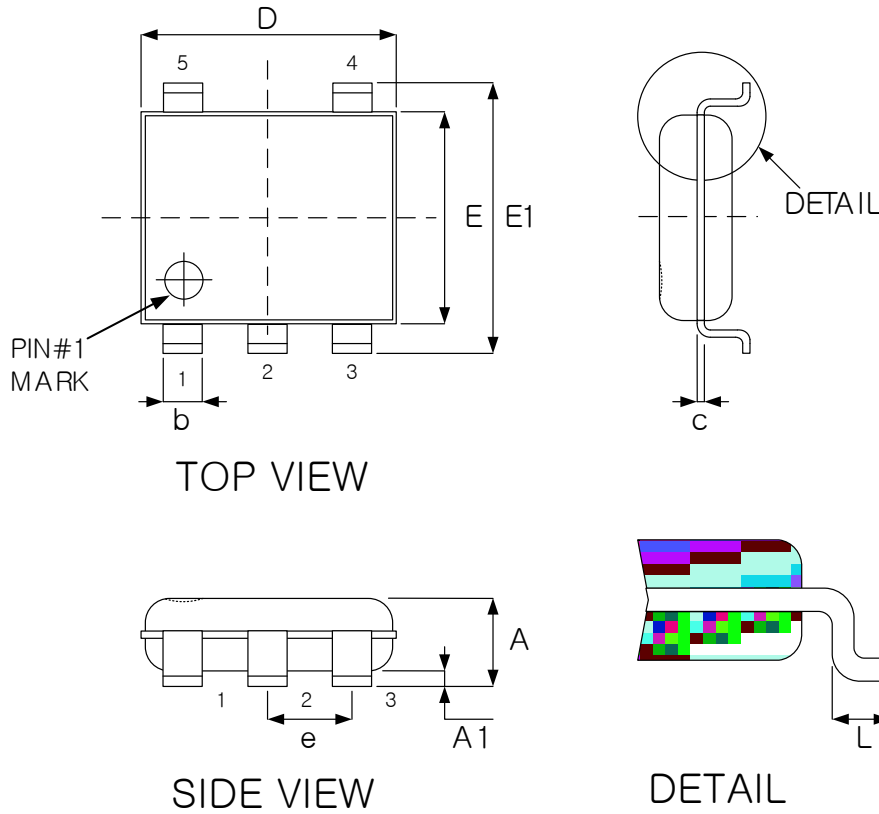
As the above equations show, it is desirable to work with ICs whose  $\theta_{JA}$  values are small such that  $T_J$  does not increase strongly with  $P_D$ . To avoid thermally overloading the EMP8130, refrain from exceeding the absolute maximum junction temperature rating of  $150^{\circ}\text{C}$  under continuous operating conditions. Overstressing the regulator with high loading currents and elevated input-to-output differential voltages can increase the IC die temperature significantly.

## Shutdown

The FC8130 enters sleep mode when the EN pin is low. When this occurs, the pass transistor, the error amplifier, and the biasing circuits, including the bandgap reference, are turned off, thus reducing the supply current to typically  $< 1\mu\text{A}$ . The low supply current makes the FC8130 best suited for battery-powered applications. The maximum guaranteed voltage at the EN pin to enter sleep mode is 0.4V. A minimum guaranteed voltage of 1.0V at the EN pin will activate the FC8130. To constantly keep the regulator on, direct connection of the EN pin to the VIN pin is allowed.

## Package Outline Drawing

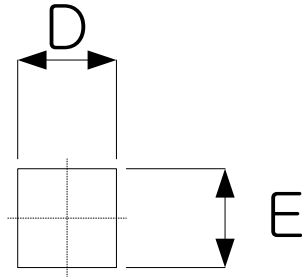
### SOT-23-5



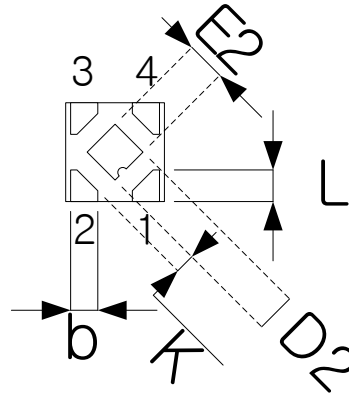
Symbol	Dimension in mm	
	Min.	Max.
A	0.90	1.45
A1	0.00	0.15
b	0.30	0.50
c	0.08	0.25
D	2.70	3.10
E	1.40	1.80
E1	2.60	3.00
e	0.95 BSC	
L	0.30	0.60

Package Outline Drawing

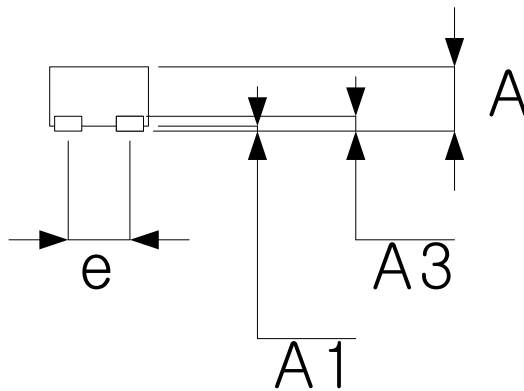
uDFN-4L (1mmx1 mm)



TOP VIEW



BOTTOM VIEW



SIDE VIEW

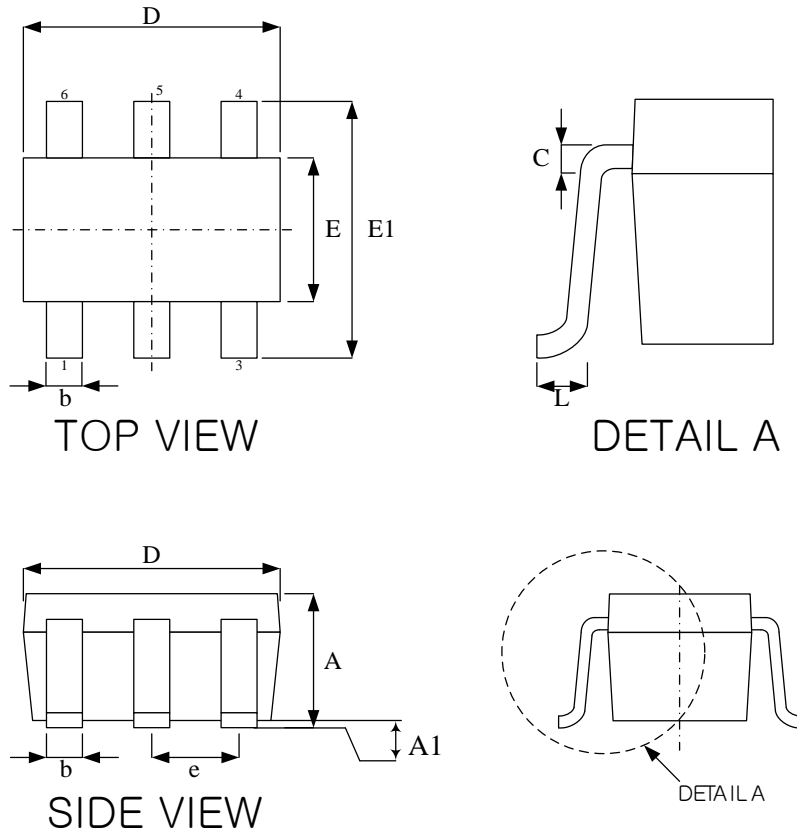
Symbol	Dimension in mm	
	Min	Max
A	0.5	0.6
A1	0	0.05
A3	0.150 REF.	
b	0.175	0.275
D	1.00 BSC	
E	1.00 BSC	
e	0.625 BSC	
L	0.2	0.5
K	0.2	-

Exposed pad

	Dimension in mm	
	Min	Max
D2	0.4	0.6
E2	0.4	0.6

## Package Outline Drawing

SC-70-5

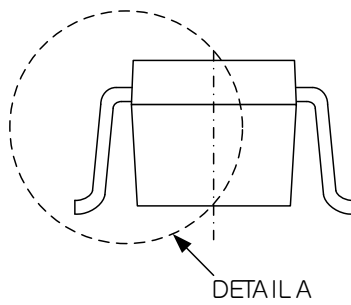
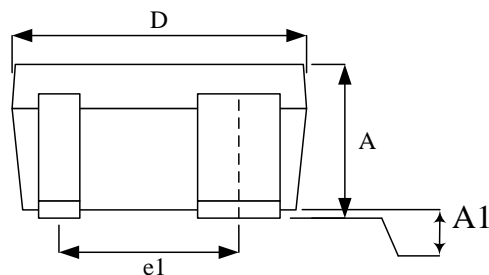
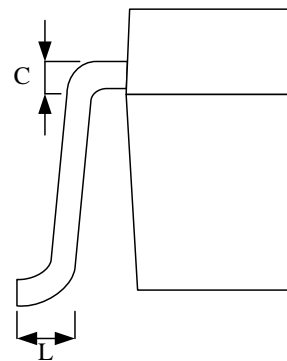
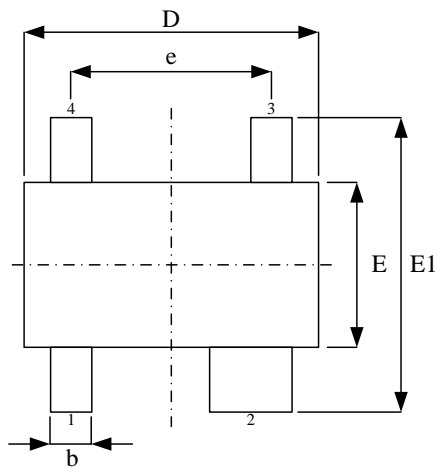


Symbol	Dimension in mm	
	Min.	Max.
A	0.80	1.10
A1	0.00	0.10
b	0.15	0.30
c	0.08	0.22
D	1.85	2.15
E	1.10	1.40
E1	1.80	2.40
e	0.65 BSC	
L	0.26	0.46

\* This drawing includes SC70 5&6 lead.  
For 5 lead packages, the No.5 was removed.

## Package Outline Drawing

SC-82-4



Symbol	Dimension in mm	
	Min.	Max.
A	0.80	1.10
A1	0.00	0.10
b	0.15	0.30
b1	0.30	0.60
c	0.08	0.22
D	1.85	2.15
E	1.10	1.40
E1	1.80	2.40
e	1.30 BSC	
e1	1.1875 BSC	
L	0.26	0.46