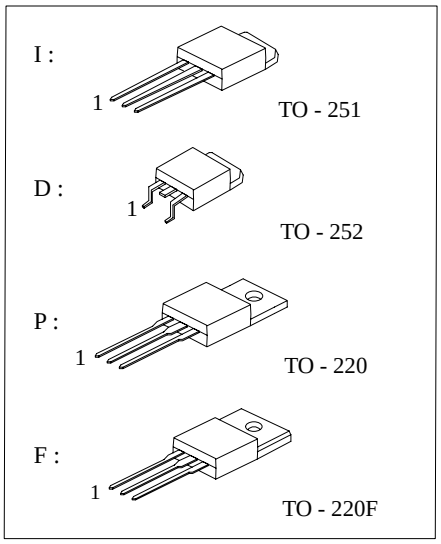
2 Amps, 650 Volts N-CHANNEL MOSFET

DESCRIPTION

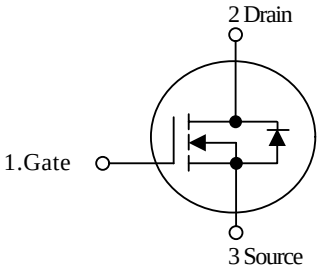
These N-Channel enhancement mode power field effect Transistors are produced using planar stripe, DMOS technology.
This advanced technology has been especially tailored to minimize on - state resistance , provide superior switching performance,and Withstand high energy pulse in the avalanche and commutaion mode .These devices are well suited for high efficiency switch mode power supply.



FEATURES

* $R_{DS(ON)}$ = 7.0Ω @V_{GS} = 10V I_D=1.2A
* Ultra Low gate charge (typical 1.5nC)
* Low reverse transfer capacitance (C_{RSS} = typical 5.0 pF)
* Fast sw itching capability
* Avalanche energy specified
* Improved dv/dt capability, high ruggedness

SYMBOL



ORDERING INFORMATION

Ordering Number	Package	Pin Assignment			Packing
		1	2	3	
FTK2N65P	TO-220	G	D	S	Tube
FTK2N65F	TO-220F	G	D	S	Tube
FTK2N65I	TO-251	G	D	S	Tube
FTK2N65D	TO-252	G	D	S	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

■ ABSOLUTE MAXIMUM RATINGS (T_C = 25℃, unless otherwise specified)

PARAMET		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	650	V
Gate-Source Voltage		V_{GSS}	±30	V
Avalanche Current (Note 2)		I_{AR}	2.0	A
Drain Current Continuous	T_C = 25°C	I_D	2.0	A
	T_C = 100°C		1.2	A
Drain Current Pulsed (Note 2)		I_{DP}	8.0	A
Avalanche Energy	Repetitive(Note 2)	E_{AR}	5.4	mJ
	Single Pulse(Note 3)	E_{AS}	131	mJ
Peak Diode Recovery		dv/dt	4.5	V/ns
Total Power Dissipation (TO-251/252/TO-220/TO-220F)	T_C = 25°C	P_D	45/45/62.5/31	W
	Derate above 25°C		0.36/0.36/0.5/0.25	W / ˚C
Junction Temperature		T_J	+150	˚C
Storage Temperature		T_{STG}	-55 ~ +150	˚C

Note:1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.
Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. Repetitive Rating: Pulse width limited by maximum junction temperature
3. L=64mH, I_{AS}=2.0A, V_{DD}=50V, R_G=25 Ω, Starting T_J = 25°C
4. I_{SD}≤ 2.0A, di/dt ≤ 300A/μs, V_{DD} ≤ BVDSS, Starting T_J = 25°C

■ THERMAL DATA

PARAMETER	PACKAGE	SYMBOL	RATINGS	UNIT
Thermal Resistance Junction-Ambient	TO-251	θ_{JA}	112	˚C / W
	TO-252		112	
	TO-220		54	
	TO-220F		54	
Thermal Resistance Junction-Case	TO-251	θ_{Jc}	2.8	
	TO-252		2.8	
	TO-220		2	
	TO-220F		4	

■ ELECTRICAL CHARACTERISTICS (T_J = 25˚C , unless Otherwise specified.)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage		BV_{DSS}	V_{GS} = 0V, I_D = 250μA	650			V
Zero Gate Voltage Drain Current		I_{DSS}	V_{DS} = 650V, V_{GS} = 0V			10	μA
Gate-Body Leakage Current	Forward	I_{GSS}	V_{GS} = 30V, V_{DS} = 0V			100	nA
	Reverse		V_{GS} = -30V, V_{DS} = 0V			-100	nA
Breakdown Voltage Temperature Coefficient		△BV_{DSS}/△T_J	I_D = 250 μA		0.7		V / ˚C
ON CHARACTERISTICS							
Gate Threshold Voltage		$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250μA	2.0		4.0	V
Static Drain-Source On-Resistance		$R_{DS(ON)}$	V_{GS} = 10V, I_D =1A			7	Ω
DYNAMIC CHARACTERISTICS							
Input Capacitance		C_{ISS}	V_{DS} =25V, V_{GS} =0V, f =1MHz		270	350	pF
Output Capacitance		C_{OSS}			40	50	pF
Reverse Transfer Capacitance		C_{RSS}			4	7	pF

■ ELECTRICAL CHARACTERISTICS (T_J = 25˚C , unless Otherwise specified.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SWITCHING CHARACTERISTICS						
Turn-On Delay Time	$t_{D(ON)}$	V_{DD} =300V, I_D =2.0A, R_G=25Ω (Note 1,2)		10		ns
Rise Time	t_R			30		ns
Turn-Off Delay Time	$t_{D(OFF)}$			30		ns
Fall Time	t_F			30		ns
Total Gate Charge	Q_G	V_{DS}=480V, V_{GS}=10V, I_D=2.0A (Note 1, 2)		10		nC
Gate-Source Charge	Q_{GS}			1.5		nC
Gate-Drain Charge	Q_{GD}			5		nC
DRAIN-SOURCE DIODE CHARACTERISTICS						
Drain-Source Diode Forward Voltage	V_{SD}	V_{GS} = 0 V, I_{SD} = 2.0 A			1.5	V
Continuous Drain-Source Current	I_{SD}				2.0	A
Pulsed Drain-Source Current	I_{SM}				8.0	A
Reverse Recovery Timee	t_{RR}	V_{GS} = 0 V, I_{SD} = 2.0A, di/dt = 100 A/μs (Note1)		250		ns
Reverse Recovery Charge	Q_{RR}			1.0		μC

Note: 1. Pulse Test: Pulse Width ≤300μs, Duty Cycle≤2%

2. Essentially Independent of Operating Temperature

■ TEST CIRCUITS AND WAVEFORMS

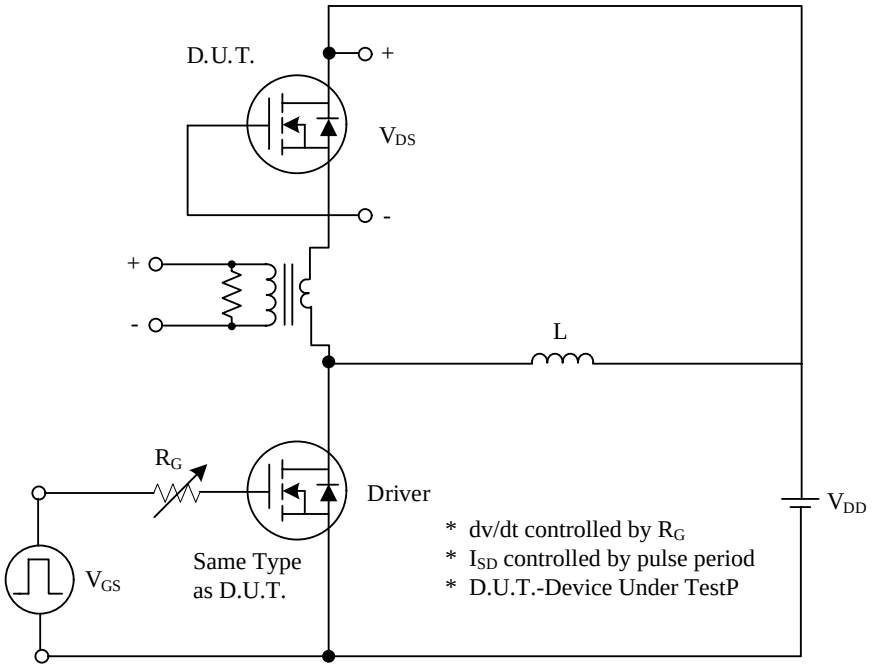


Fig. 1A Peak Diode Recovery dv/dt Test Circuit

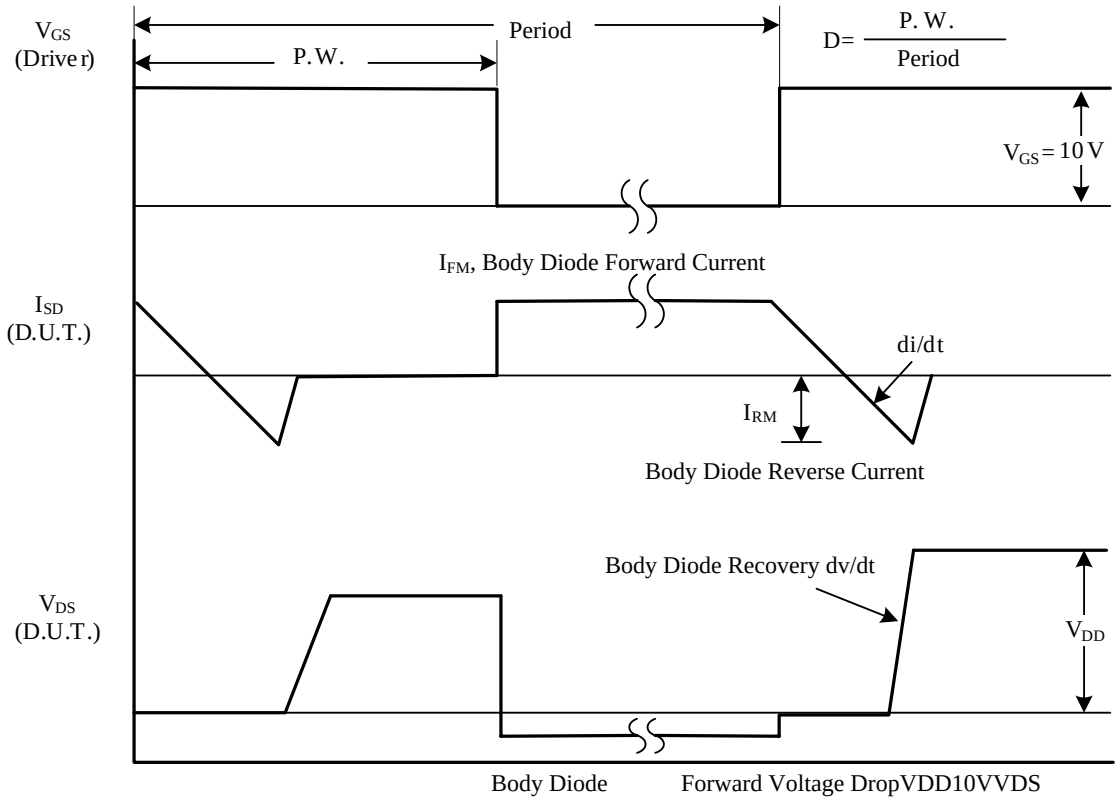


Fig. 1B Peak Diode Recovery dv/dt Waveforms

■ TEST CIRCUITS AND WAVEFORMS (Cont.)

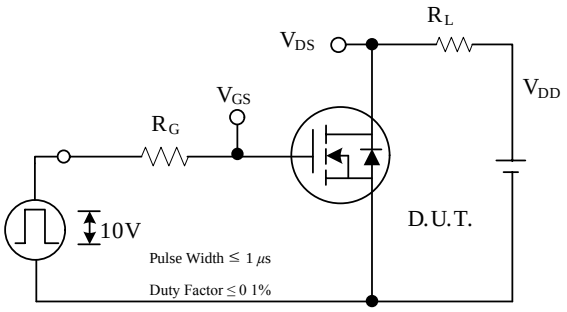


Fig. 2A Switching Test Circuit

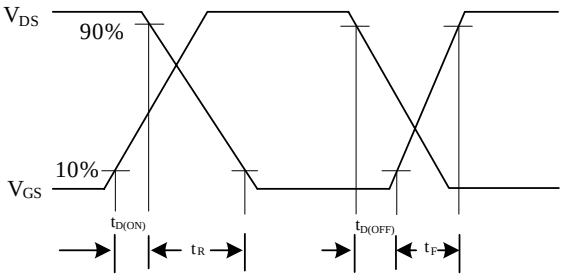


Fig. 2B Switching Waveforms

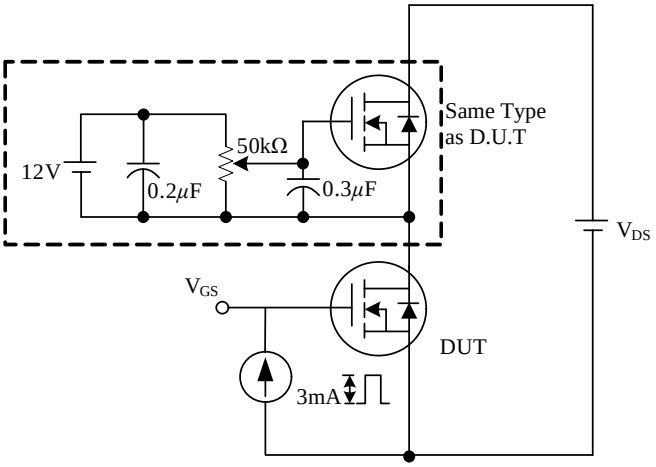


Fig. 3A Gate Charge Test Circuit

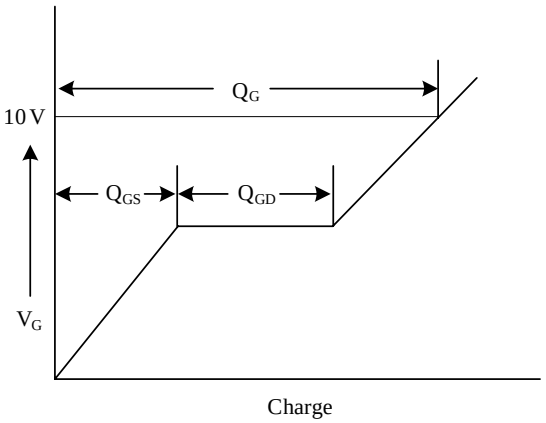


Fig. 3B Gate Charge Waveform

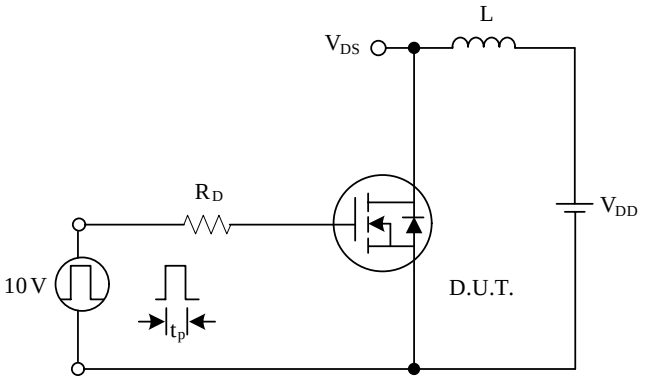


Fig. 4A Unclamped Inductive Switching Test Circuit

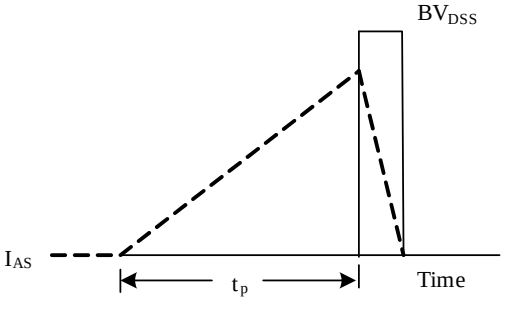


Fig. 4B Unclamped Inductive Switching Waveforms

■ TYPICAL CHARACTERISTICS

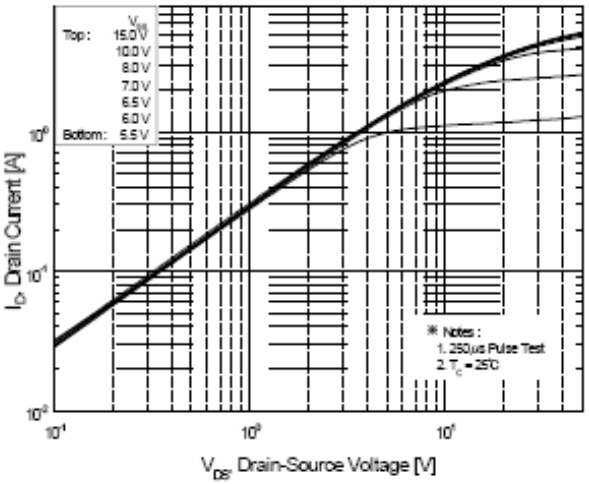


Figure 1. On-Region Characteristics

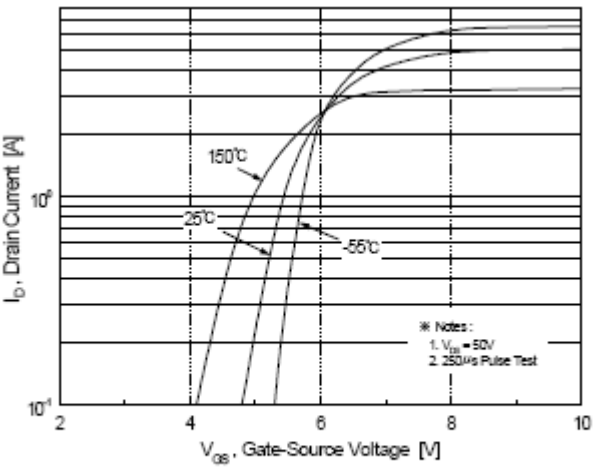


Figure 2. Transfer Characteristics

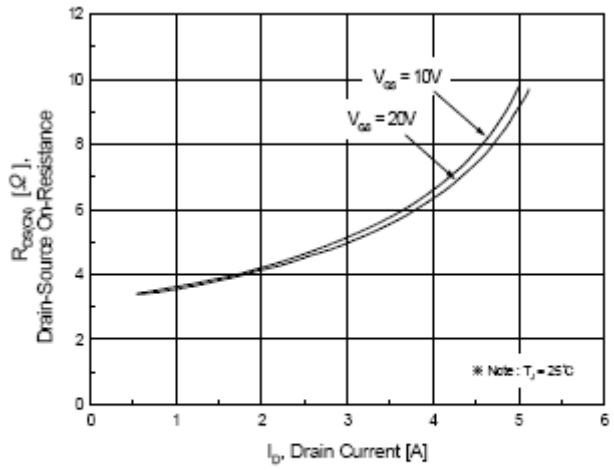


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

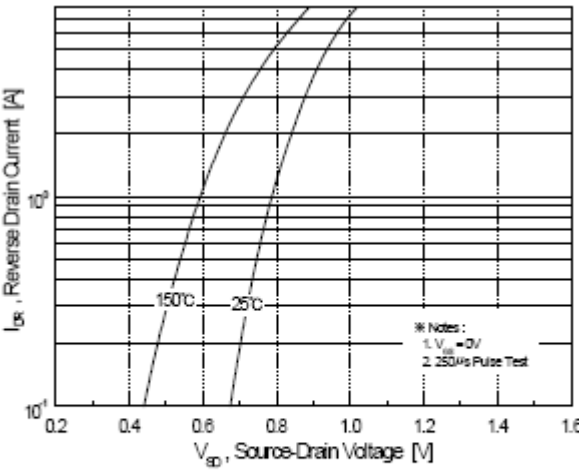


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

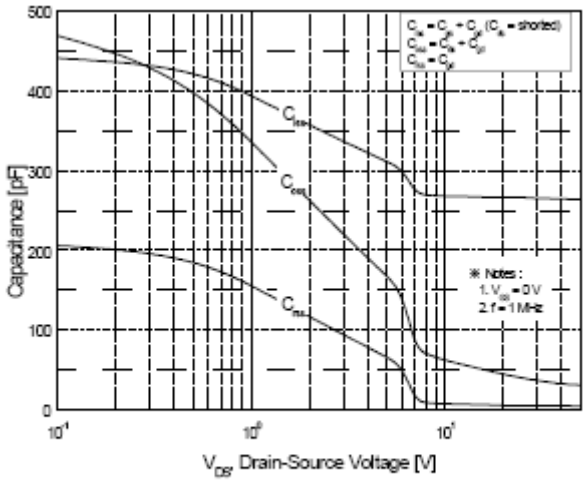


Figure 5. Capacitance Characteristics

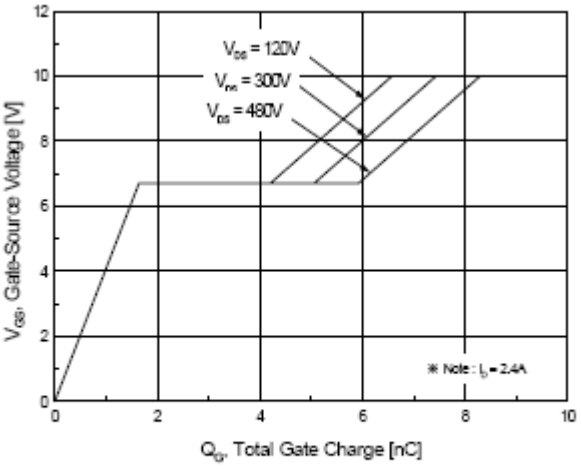


Figure 6. Gate Charge Characteristics

■ **TYPICAL CHARACTERISTICS(Cont.)**

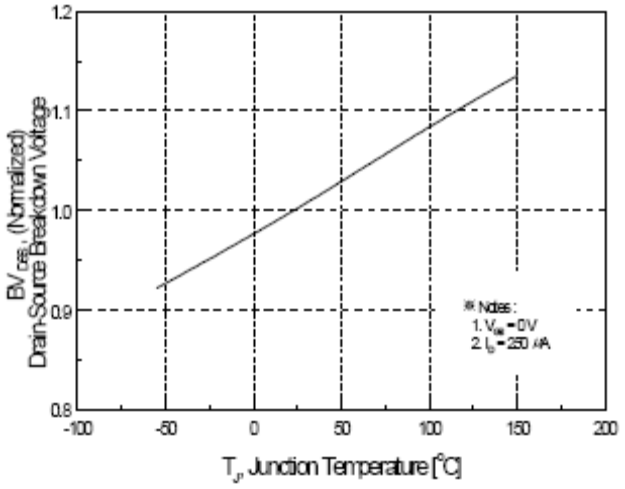


Figure 7. Breakdown Voltage Variation vs. Temperature

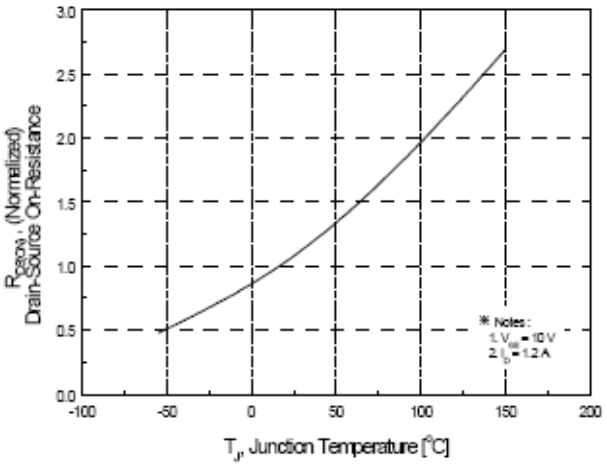


Figure 8. On-Resistance Variation vs. Temperature

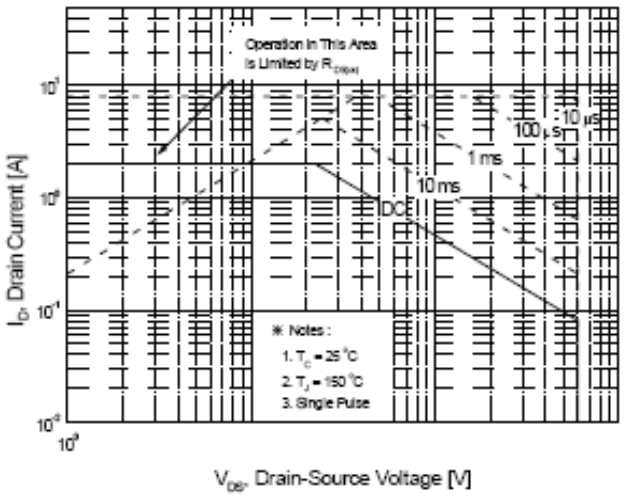


Figure 9. Maximum Safe Operating Area

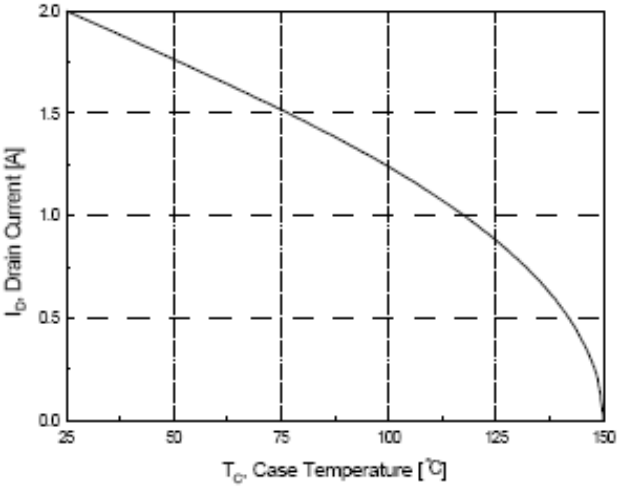


Figure 10. Maximum Drain Current vs. Case Temperature

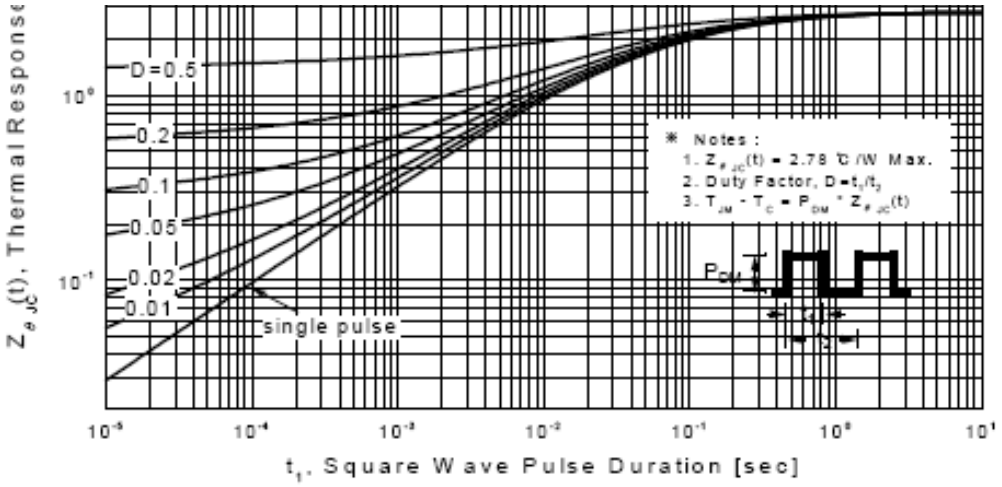


Figure 11. Transient Thermal Response Curve