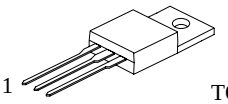
6.0A, 400V, 1.0Ω
N-CHANNEL POWER MOSFET

Power MOS FET

■ DESCRIPTION

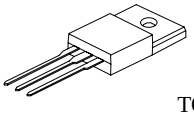
- IRF730 is 400V High voltage N-Channel enhancement mode power MOS-FET chip fabricated in advanced silicon epitaxial planar technology;
- Advanced termination scheme to provide enhanced voltage-blocking capability;
- Avalanche Energy Specified;
- Source-to-Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode;
- IRF730 product is widely used in AC-DC power suppliers, DC-DC converters and H-bridge PWM motor drivers.

P :



1 TO - 220

F :

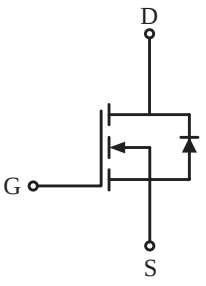


1 TO - 220F

■ FEATURES

* 6.0A, 400V, $R_{DS(ON)}$=1.0Ω
* Single Pulse Avalanche EnergyRated
* Rugged - SOA is Power Dissipation Limited
* Fast Switching Speeds
* Linear Transfer Characteristics
* High Input Impedance

■ SYMBOL



■ ORDERING INFORMATION

Ordering Number	Package	Pin Assignment			Packing
		1	2	3	
IRF730	TO-220	G	D	S	Tube
IRF730F	TO-220F	G	D	S	Tube

Note: Pin Assignment: G: Gate D: Drain S: Source

■ ABSOLUTE MAXIMUM RATINGS (Ta = 25˚C, unless otherwise specified)

PARAMET		SYMBOL	RATINGS	UNIT
Drain-Source Voltage (TJ = 25˚C ~ 125˚C)		VDS	400	V
Drain to Gate Voltage (RGS = 20kΩ) (TJ =25˚C ~ 125˚C)		VDGR	400	V
Gate to Source Voltage		IGS	±20	V
Drain Current	Continuous	ID	5.5	A
	TC = 100°C	ID	3.5	A
	Pulsed	IDM	22	A
Maximum Power Dissipation		PD	74	W
Derating above 25℃			0.6	W/˚C
Single Pulse Avalanche Energy Rating (VDD=50V, starting TJ =25˚C, L=16mH, RG=25Ω, peak IAS = 5.5A)		EAS	290	mJ
Juction Temperature		TJ	-55~ +150	˚C
Storage Temperature		TSTG	-55~ +150	˚C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Thermal Resistance Junction-Ambient	θ_{JA}	62	˚C / W
Thermal Resistance Junction-Case	θ_{Jc}	1.7	

■ ELECTRICAL CHARACTERISTICS (TC = 25˚C , unless Otherwise specified.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Drain-Source Breakdown Voltage	BVDSS	ID = 250μA, VGS = 0V	400			V
Gate to Threshold Voltage	VGS(THR)	VDS = VGS, ID = 250μA	2.0		4.0	V
On-State Drain Current (Note 1)	ID(ON)	VDS > ID(ON) X RDS(ON)MAX, VGS = 10V	5.5			A
Zero Gate Voltage Drain Current	IDSS	VDS = Rated BVDSS, VGS = 0V			25	μA
		VDS = 0.8 x Rated BVDSS, VGS = 0V, TJ = 125˚C			250	μA
Gate to Source Leakage Current	IGSS	VDS = ±20V			±100	nA
Drain to Source On Resistance (Note 1)	RDS(ON)	ID = 3.3A, VGS = 10V		0.85	1.0	Ω
Forward Transconductance (Note 1)	gFS	VDS ≥ 10V, ID = 3.3A	2.9	4.4		S
Turn-On Delay Time	tDLY(ON)	VDD = 200V, ID ≈ 3.5A, RGS = 12Ω, RL = 57Ω MOSFET Switching Times are Essentially Independent of Operating Temperature		10		ns
Rise Time	tR			15		ns
Turn-Off Delay Time	tDLY(OFF)			38		ns
Fall Time	tF			14		ns
Total Gate Charge (Gate to Source + Gate to Drain)	QG(TOT)	VGS = 10V, ID = 3.5A, VDS = 0.8 X Rated BVDSS IG(REF) = 1.5mA Gate Charge is Essentially Independent of Operating Temperature			38	nC
Gate to Source Charge	QGS				5.7	nC
Gate to Drain “Miller” Charge	QGD				22	nC
Input Capacitance	CISS	VDS = 25V, VGS = 0V,f = 1MHz		700		pF
Output Capacitance	COSS			170		pF
Reverse - Transfer Capacitance	CRSS			64		pF

■ ELECTRICAL CHARACTERISTICS(Cont.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SOURCE TO DRAIN DIODE SPECIFICATIONS						
Source to Drain Diode Voltage (Note 1)	V_{SD}	T_J = 25°C, I_{SD} =5.5A, V_{GS} = 0V			1.6	V
Continuous Source to Drain Current	I_S				5.5	A
Pulse Source to Drain Current(Note 2)	I_{SM}				22	A
Reverse Recovery Time	t_{RR}	T_J = 25°C, I_{SD} =3.5A,		270		ns
Reverse Recovery Charge	Q_{RR}	dI_{SD}/dt =100 A/μs		1.8		μC

Note:

1. Pulse Test: Pulse width ≤ 300μs, Duty cycle ≤ 2%
2. Repetitive rating: Pulse width limited by maximum junction temperature.

■ TEST CIRCUITS AND WAVEFORMS

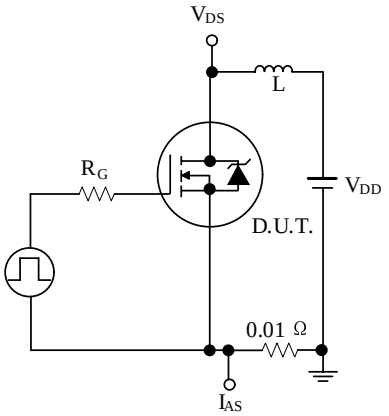


Figure 1A. Unclamped Energy Test Circuit

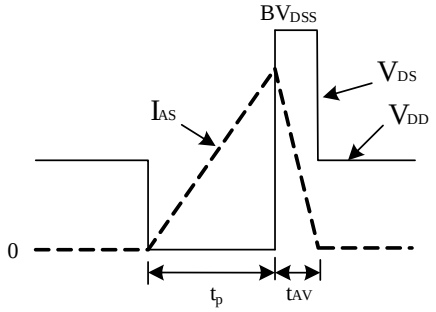


Figure 1B. Unclamped Energy Waveforms

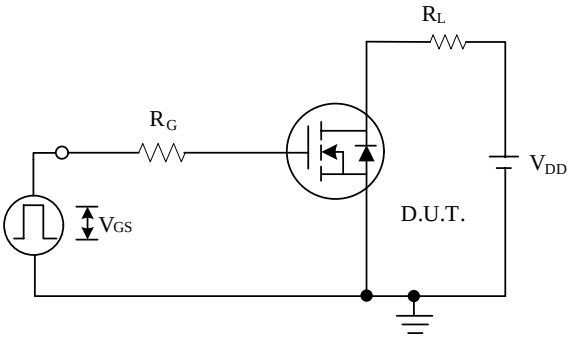


Figure 2A. Switching Time Test Circuit

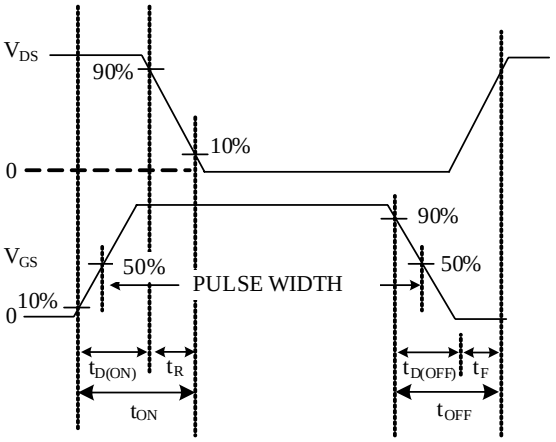


Figure 2B. Resistive Switching Waveforms

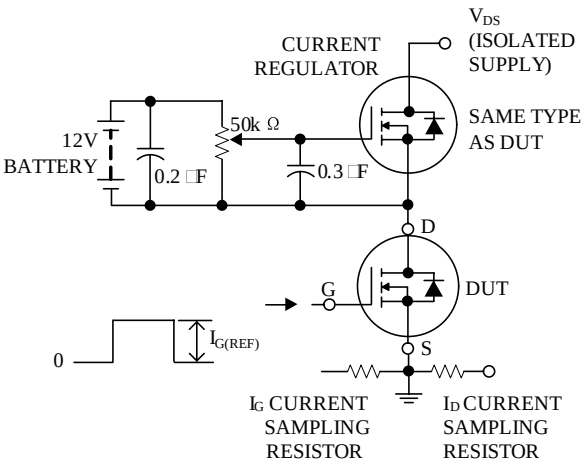


Figure 3A. Gate Charge Test Circuit

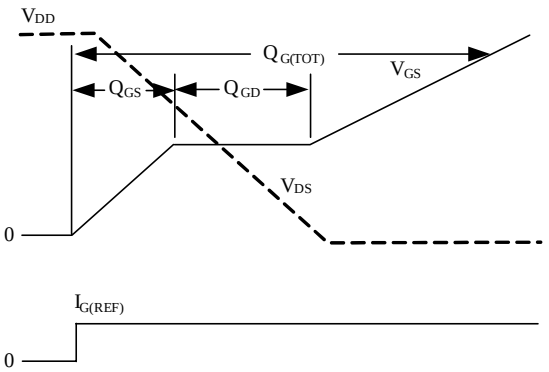
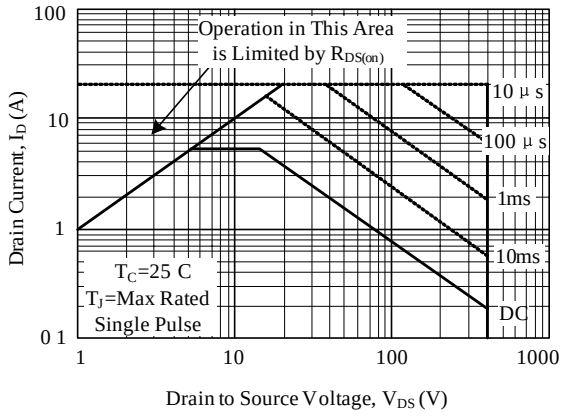


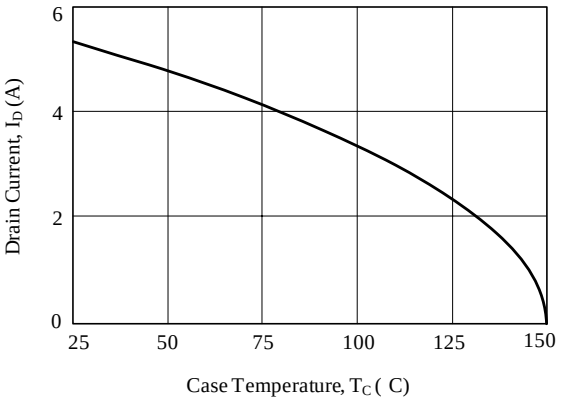
Figure 3B. Gate Charge Waveforms

■ TYPICAL PERFORMANCE CUVES (Unless Otherwise Specified)

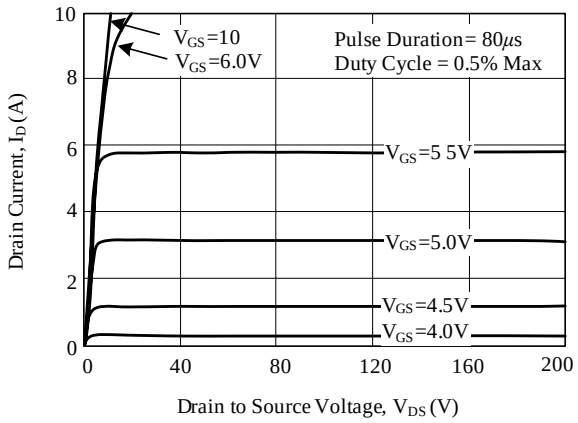
Forward Bias Safe Operating Area



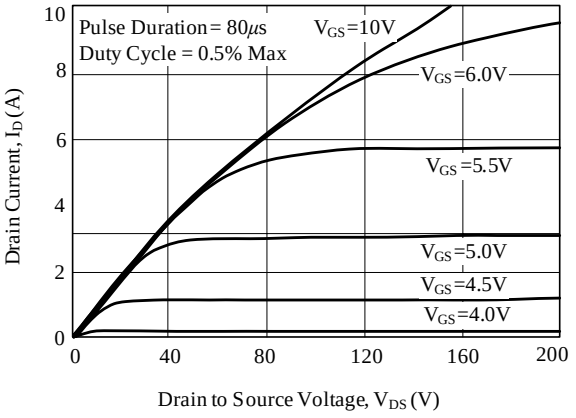
Maximum Contionuous Drain Current vs. Case Temperature



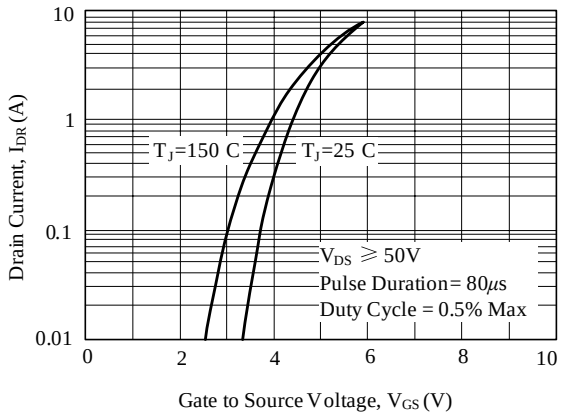
Output Characteristics



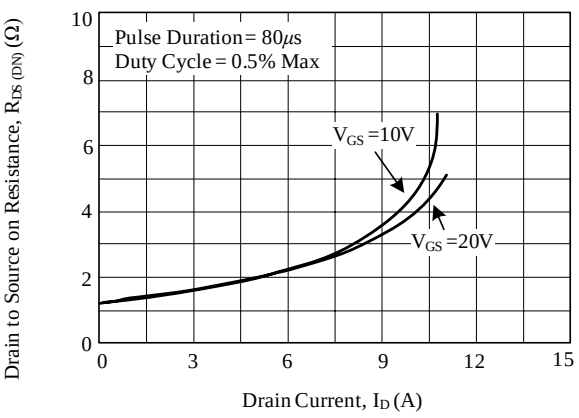
Sturation Characteristics



Transfer Characteristics

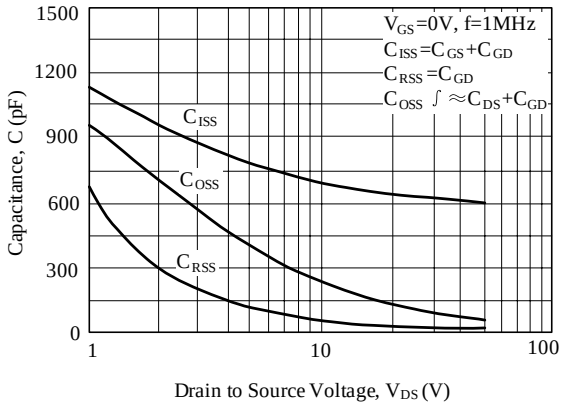


Drain to Source on Resistance vs. Gate Voltage and Drain Current

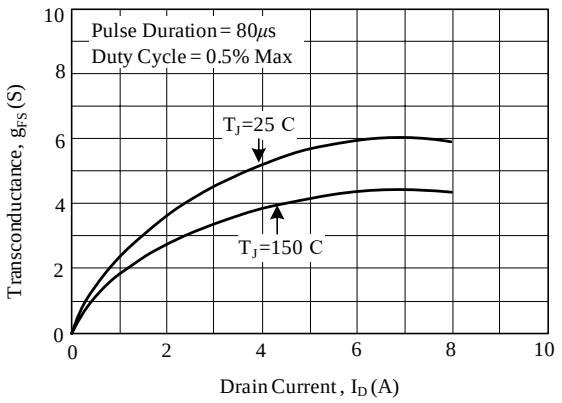


■ TYPICAL PERFORMANCE CUVES

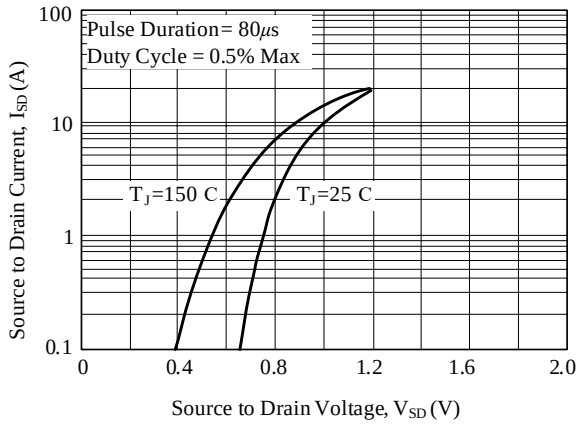
Capacitance vs. Drain to Source Voltage



Transconductance vs. Drain Current



Source to Drain Diode Voltage



Gate to Source Voltage vs. Gate Charge