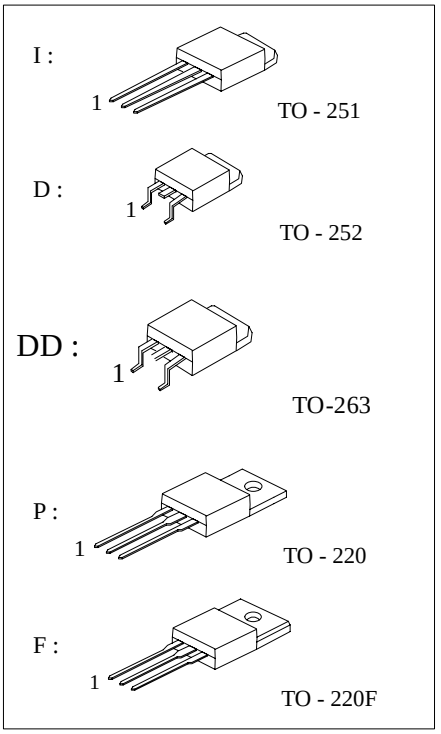
4.4A, 500V, 1.5Ω
N-CHANNEL POWER MOSFET

Power MOSFET



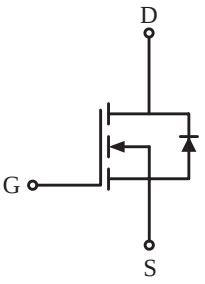
■ DESCRIPTION

- FTK5N50 is 500V High voltage N-Channel enhancement mode power MOS-FET chip fabricated in advanced silicon epitaxial planar technology;
- Advanced termination scheme to provide enhanced voltage-blocking capability;
- Avalanche Energy Specified;
- Source-to-Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode;
- FTK5N50 product is widely used in AC-DC power suppliers, DC-DC converters and H-bridge PWM motor drivers.

■ FEATURES

* 4.4A, 500V, $R_{DS(ON)}$=1.5Ω
* Single Pulse Avalanche Energy Rated
* Rugged - SOA is Power Dissipation Limited
* Fast Switching Speeds
* Linear Transfer Characteristics
* High Input Impedance

■ SYMBOL



■ ORDERING INFORMATION

Ordering Number	Package	Pin Assignment			Packing
		1	2	3	
FTK5N50P	TO-220	G	D	S	Tube
FTK5N50F	TO-220F	G	D	S	Tube
FTK5N50DD	TO-263	G	D	S	Tape Reel
FTK5N50I	TO-251	G	D	S	Tube
FTK5N50D	TO-252	G	D	S	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

■ ABSOLUTE MAXIMUM RATINGS (T_a = 25˚C, unless otherwise specified)

PARAMET		SYMBOL	RATINGS	UNIT
Drain to Source Voltage (T_J = 25˚C ~ 125˚C)		V_{DS}	500	V
Drain to Gate Voltage (R_{GS} = 20kΩ) (T_J =25˚C ~ 125˚C)		V_{DGR}	500	V
Gate to Source Voltage		I_{GS}	±30	V
Drain Current	Continuous	I_D	4.4	A
	T_a = 100°C	I_D	2.8	A
	Pulsed	I_{DM}	17.6	A
Maximum Power Dissipation (TO-251/252/TO-220F/220/263)	T_C = 25°C	P_D	45/45/31/62.5	W
	Derating above 25℃		0.36/0.36/0.25/0.5	W/˚C
Single Pulse Avalanche Energy Rating (V_{DD}=50V, starting T_J =25℃,L=19.7mH,Rg =25Ω, peak I_{AS} =5.0A)		E_{AS}	270	mJ
Junction Temperature		T_J	+150	˚C
Storage Temperature		T_{STG}	-55 ~ +150	˚C

Note: 1. Signified recommend operating range that indicates conditions for which the device is intended to be functional, but does not guarantee specific performance limits.
2. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ ELECTRICAL CHARACTERISTICS (T_C = 25˚C , unless Otherwise specified.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 250μA, V_{GS} = 0V	500			V
Gate to Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250μA	2.0		4.0	V
On-State Drain Current (Note 1)	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ X $R_{DS(ON)MAX}$, V_{GS} = 10V	4.5			A
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Rated BV_{DSS}, V_{GS} = 0V			1	μA
		V_{DS} = 0.8 x Rated BV_{DSS}, V_{GS} = 0V, T_J = 125˚C			10	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±20V			±100	nA
Drain to Source On Resistance (Note 2)	$R_{DS(ON)}$	I_D = 2.5A, V_{GS} = 10V		1.15	1.5	Ω
Forward Transconductance (Note 2)	g_{FS}	V_{DS} ≥ 10V, I_D = 2.5A	2.5	4.2		S
Turn-On Delay Time	$t_{DLY(ON)}$	V_{DD} = 250V, I_D ≈ 2.5A, R_{GS} = 25Ω, R_L = 50Ω (Note 2)		23		ns
Rise Time	t_R			17		ns
Turn-Off Delay Time	$t_{DLY(OFF)}$			40		ns
Fall Time	t_F			13		ns
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 10V, I_D = 5A, V_{DS} = 0.8 X Rated BV_{DSS} $I_{G(REF)}$ = 1.5mA (Note 3)		12		nC
Gate to Source Charge	Q_{GS}			3.4		nC
Gate to Drain “Miller” Charge	Q_{GD}			4.5		nC
Input Capacitance	C_{ISS}	V_{DS} = 25V, V_{GS} = 0V,f = 1.0MHz		510		pF
Output Capacitance	C_{OSS}			69		pF
Reverse - Transfer Capacitance	C_{RSS}			6		pF

Note: 1. Pulse Test: Pulse width ≤ 300μs, Duty cycle ≤ 2%
2. MOSFET Switching Times are Essentially Independent of Operating Temperature.
3. Gate Charge is Essentially Independent of Operating Temperature.

■ ELECTRICAL CHARACTERISTICS (Cont.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SOURCE TO DRAIN DIODE SPECIFICATIONS						
Source to Drain Diode Voltage (Note 1)	V_{SD}	T_J = 25°C, I_{SD} = 5A, V_{GS} = 0V			1.4	V
Continuous Source to Drain Current	I_{SD}	Note 2			5.0	A
Pulse Source to Drain Current	I_{SDM}				20	A
Reverse Recovery Time	t_{RR}	T_J = 25°C, I_{SD} = 5A,		300		ns
Reverse Recovery Charge	Q_{RR}	dI_{SD}/dt =100 A/μs		3.1		μC

Note:

1. Pulse Test: Pulse width ≤ 300μs, Duty cycle ≤ 2%
2. Modified MOSFET symbol showing the integral reverse P-N junction diode as below.

■ TEST CIRCUITS AND WAVEFORMS

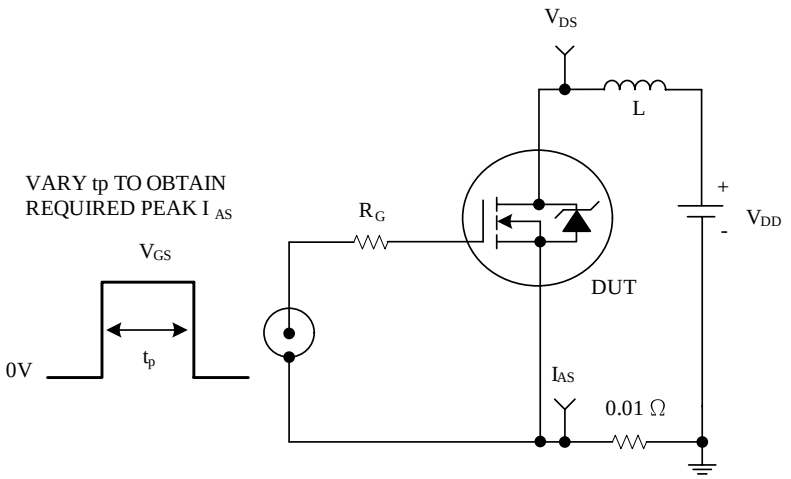


FIGURE 1. UNCLAMPED ENERGY TEST CIRCUIT

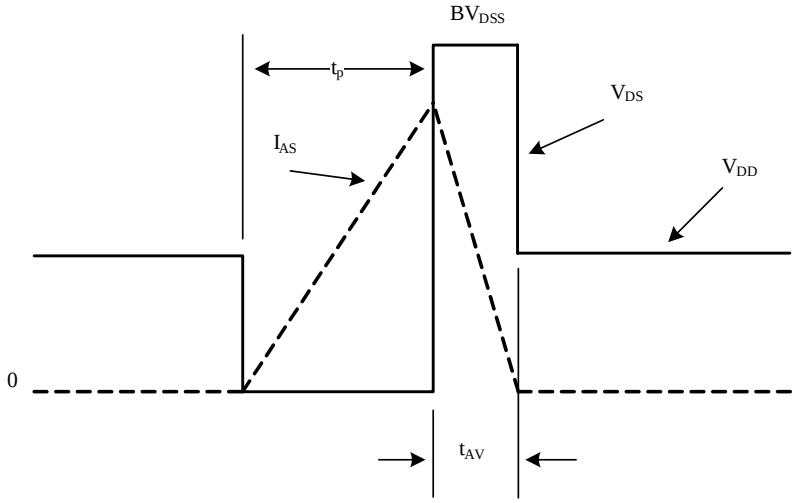


FIGURE 2. UNCLAMPED ENERGY WAVEFORMS

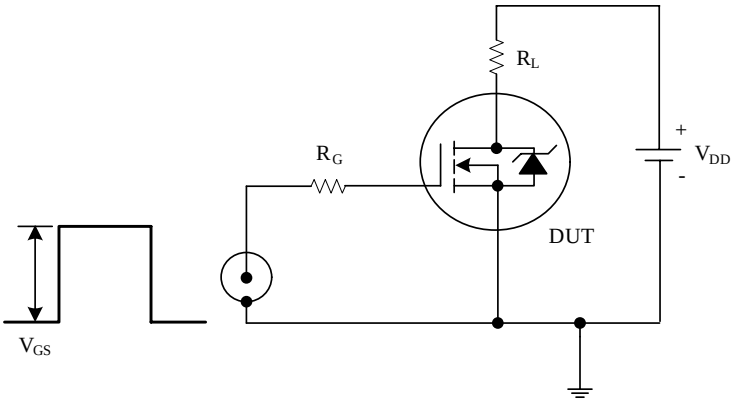


FIGURE 3. SWITCHING TIME TEST CIRCUIT

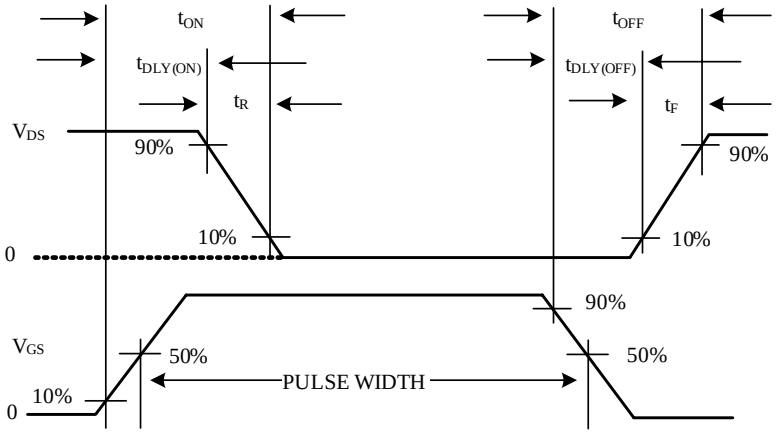


FIGURE 4. RESISTIVE SWITCHING WAVEFORMS

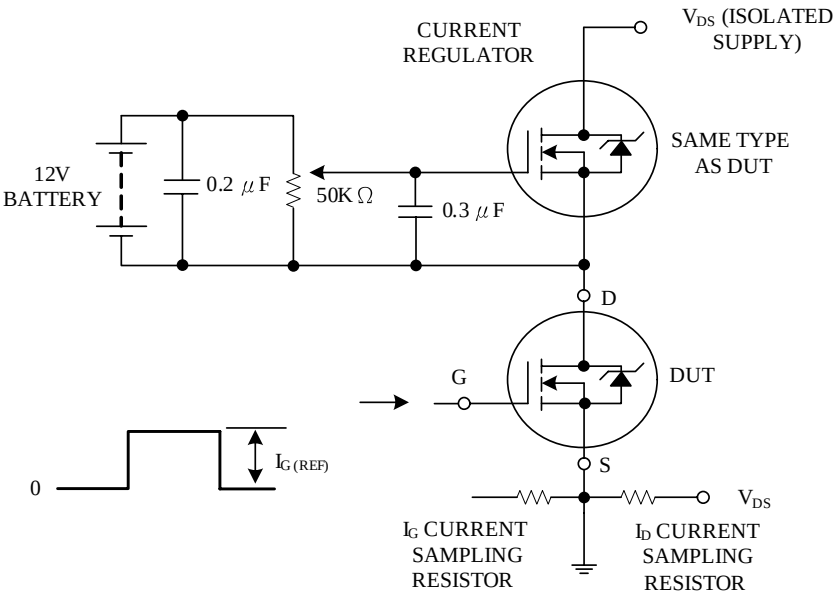


FIGURE 5. GATE CHARGE TEST CIRCUIT

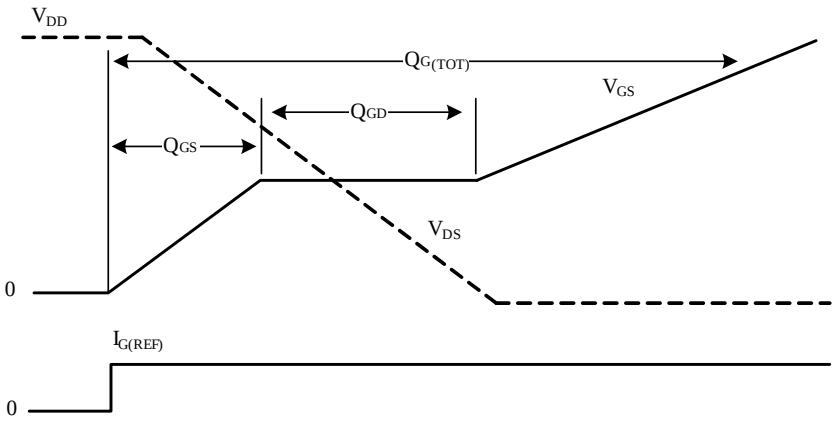


FIGURE 6. GATE CHARGE WAVEFORMS

Fig1. I_D - V_{DS}

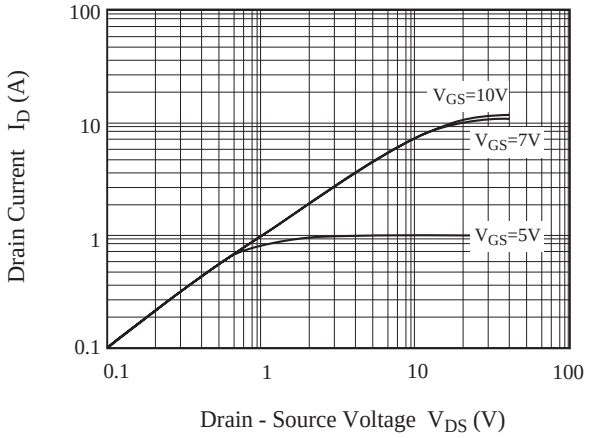


Fig2. I_D - V_{GS}

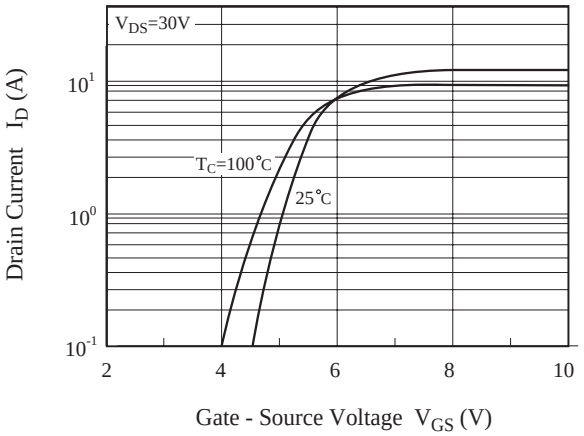


Fig3. BV_{DSS} - T_j

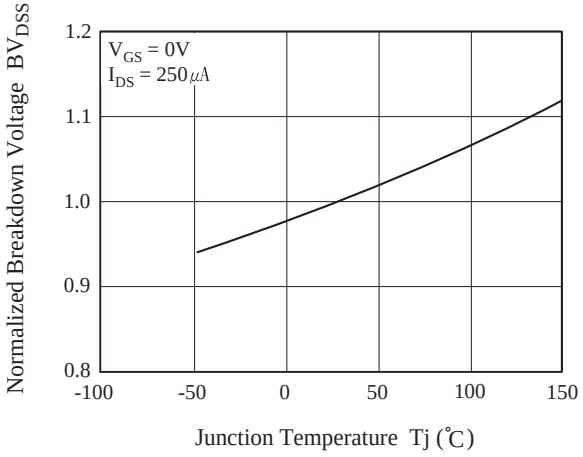


Fig4. $R_{DS(ON)}$ - I_D

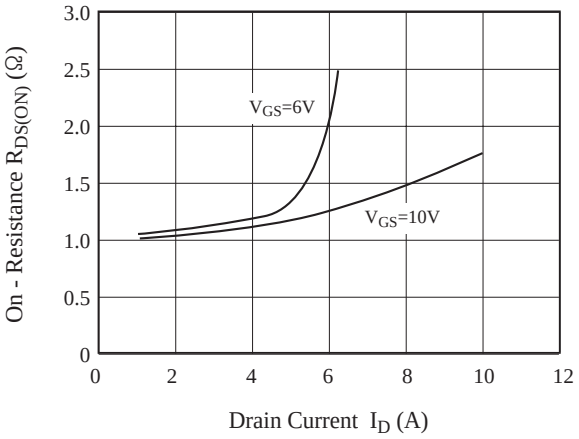


Fig5. I_S - V_{SD}

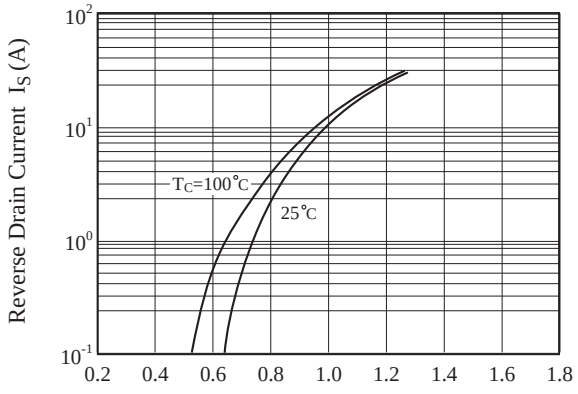


Fig6. $R_{DS(ON)}$ - T_j

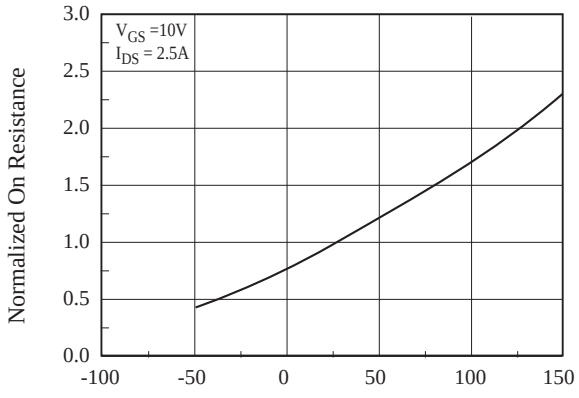


Fig 7. C - V_{DS}

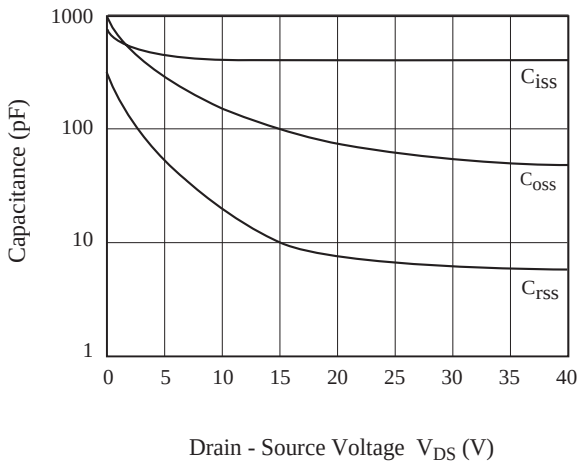


Fig8. Q_g- V_{GS}

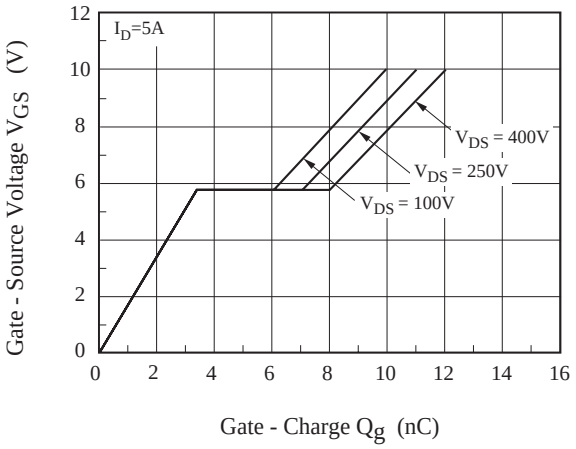


Fig9. Safe Operation Area

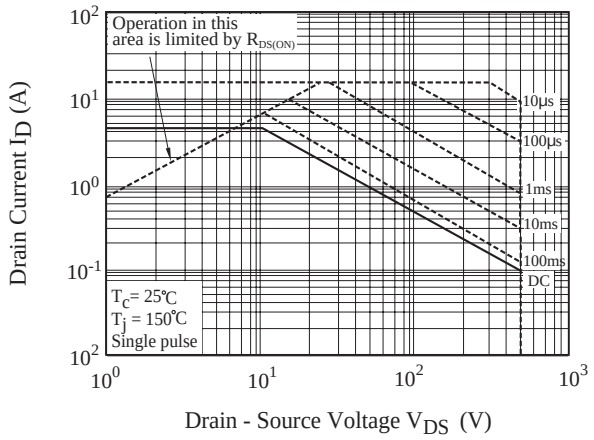


Fig10. I_D - T_j

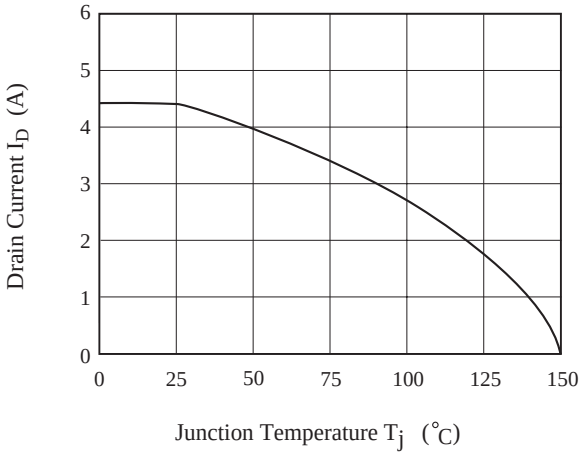


Fig11. Transient Thermal Response Curve